Customer Number: 23624

WHAT IS CLAIMED IS:

1. An FIR filter apparatus comprising:

a coefficient generator to generate first and second coefficients;

a first control conductor;

a second control conductor;

a controller coupled to a first end of said first control conductor and a first end of said second control conductor;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller; and

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

2. An apparatus according to Claim 1,

wherein said coefficient generator generates a third coefficient,

wherein said apparatus further comprises:

a second delay circuit responsive to said first delay circuit;

a third control conductor, wherein a first end of said third control conductor is coupled to said controller;

a third memory coupled to the second end of said shared wiring and coupled to a second end of said third control conductor to store the third coefficient in response to said controller;

a third multiplier responsive to the third coefficient stored in said third memory and said second delay element.

3. An apparatus according to Claim 2, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay, wherein the first time delay is equal to the second time delay.

4. An apparatus according to Claim 2, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay, wherein the first time delay is different than the second time delay.

5. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said coefficient generator;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

6. An apparatus according to Claim 5, further comprising a controller to synchronize said coefficient generator with each of said N memories.

7. An apparatus according to Claim 6,further comprising a control wiring comprising N conductors, wherein a first end of each of said N conductors being coupled to said controller and a second end of each of said N conductors being coupled to a respective one of said N memories.

8. An apparatus according to Claim 7, wherein said shared wiring comprises M conductors, M being a positive integer greater than 2, and wherein said coefficient is M bits wide.

9. An FIR filter apparatus comprising:

a coefficient generator to generate first and second coefficients;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a selector;

a first memory coupled to a second end of said shared wiring to store the first coefficient in response to said selector;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring to store the second coefficient in response to said selector;

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

10. An apparatus according to Claim 9,

wherein said coefficient generator generates a third coefficient,

wherein said apparatus further comprises:

a second delay circuit responsive to said first delay circuit;

a third memory coupled to the second end of said shared wiring to store the third coefficient in response to said selector;

a third multiplier responsive to the third coefficient stored in said third memory and said second delay element.

11. An apparatus according to Claim 10, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay, wherein the first time delay is equal to the second time delay.

12. An apparatus according to Claim 10, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay,

wherein the first time delay is different than the second time delay.

13. An apparatus according to Claim 9, wherein said selector comprises a shift register and a multiplexer.

14. An apparatus according to Claim 13, wherein an input of said shift register is coupled to an output of said multiplexer, wherein an output of said shift register is coupled to a first input of said multiplexer, and wherein a second input of said multiplexer is coupled to an asserted signal.

15. An apparatus according to Claim 14, further comprising

an initialization controller coupled to said coefficient generator; and

an initialization conductor, a first end being coupled to said initialization controller and a second end being coupled to a selector input of said multiplexer.

16. An apparatus according to Claim 9, further comprising

an initialization controller coupled to said coefficient generator; and

an initialization conductor, a first end being coupled to said initialization controller and a second end being coupled to said selector.

17. An apparatus according to Claim 14, wherein said shift register comprises a first register coupled to said first memory and a second register coupled to said second memory.

18. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said coefficient generator;

a selector;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients in response to said selector; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

19. An apparatus according to Claim 18, further comprising an initialization controller to synchronize said coefficient generator with each of said N memories.

20. An apparatus according to Claim 19, further comprising an initialization conductor coupled to said initialization controller and said selector.

21. An apparatus according to Claim 18, wherein said shared wiring comprises M conductors, M being a positive integer greater than 2, wherein said coefficient is M bits wide.

22. An apparatus according to Claim 18, wherein said selector comprises a shift register and a multiplexer.

23. An apparatus according to Claim 22, wherein an input of said shift register is coupled to an output of said multiplexer, wherein an output of said shift register is coupled to a first input of said multiplexer, and wherein a second input of said multiplexer being coupled to an asserted signal.

24. An FIR filter according to Claim 23, further comprising:

an initialization controller coupled to said coefficient generator; and

an initialization wiring, a first end being coupled to said initialization controller and a second end being coupled to a selector input of said multiplexer.

25. An FIR filter according to Claim 22, wherein said shift register comprises N registers each corresponding to a respective one of said N memories.

26. An FIR filter apparatus comprising:

coefficient generator means for generating first and second coefficients;

controller means for synchronizing said coefficient generator;

first control conductor means for transferring a first control signal from said controller means;

second control conductor means for transferring a second control signal from said controller means;

shared wiring means for transferring the

first and second coefficients from said coefficient generator means;

input means for inputting a signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to said first control signal transferred by said first control conductor means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means in response to said second control signal transferred by said second control conductor means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

27. An apparatus according to Claim 26,

wherein said coefficient generator means generates a third coefficient,

wherein said apparatus further comprises:

third control conductor means for transferring a third control signal from said controller means

second delay means for delaying the signal from said first delay means

third memory means for storing the third coefficient transferred by said shared wiring means in response to said third control signal transferred by said third control conductor means; and

third multiplier means for multiplying the

third coefficient stored in said third memory means by the signal delayed by said second delay means.

28. An apparatus according to Claim 27, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is equal to the second time delay.

29. An apparatus according to Claim 27, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is different than the second time delay.

30. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

N memory means, each of said memory means responsive to said shared wiring means for storing a respective one of the N coefficients; and

FIR filter means for filtering an input signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.

31. An apparatus according to Claim 30, further comprising controller means for synchronizing said coefficient generator means with each of said N memory

means.

32. An apparatus according to Claim 31, further comprising control wiring means comprising N conductor means, wherein a first end of each of said N conductor means being coupled to said controller means and a second end of each of said N conductor means being coupled to a respective one of said N memory means.

33. An apparatus according to Claim 32, wherein said shared wiring means comprises M conductor means, M being a positive integer greater than 2, and wherein said coefficient is M bits wide.

34. An FIR filter apparatus comprising:

coefficient generator means for generating first and second coefficients;

shared wiring means for transferring the first and second coefficients from said coefficient generator means;

input means for inputting a signal;

selector means for providing a selector signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to the selector signal from said selector means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means

in response to the selector signal from said selector means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

35. An apparatus according to Claim 34,

wherein said coefficient generator means generates a third coefficient,

wherein said apparatus further comprises:

second delay means for delaying an output from said first delay means;

third memory means for storing the third coefficient transferred by said shared wiring means to store the third coefficient in response to said selector means;

third multiplying means for multiplying the third coefficient stored in said third memory means by the signal delayed by said second delay element.

36. An apparatus according to Claim 35, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is equal to the second time delay.

37. An apparatus according to Claim 35, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is different than the second time delay.

38. An apparatus according to Claim 34, wherein said selector means comprises a shift register and a

multiplexer.

39. An apparatus according to Claim 38, wherein an input of said shift register is coupled to an output of said multiplexer, wherein an output of said shift register is coupled to a first input of said multiplexer, and wherein a second input of said multiplexer is coupled to an asserted signal.

40. An apparatus according to Claim 39, further comprising

initialization controller means for generating an initialization signal to said coefficient generator means; and

initialization conductor means for transferring the initialization signal to a selector input of said multiplexer.

41. An apparatus according to Claim 34, further comprising

initialization controller means for generating an initialization signal to said coefficient generator means; and

initialization conductor means for transferring the initialization signal to said selector means.

42. An apparatus according to Claim 39, wherein said shift register comprises first register means coupled to said first memory means and second register means coupled to said second memory means.

43. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

selector means for generating a selection signal;

N memory means, each of said memory means for storing a corresponding one of the N coefficients transferred by said shared wiring means in response to the selection signal from said selector means; and

FIR filter means for filtering a signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.

44. An apparatus according to Claim 43, further comprising initialization controller means for synchronizing said coefficient generator means with each of said N memory means.

45. An apparatus according to Claim 44, further comprising initialization conductor means for transferring an output of said initialization controller means to said selector means.

46. An apparatus according to Claim 43, wherein said shared wiring means comprises M conductor means, M being a positive integer greater than 2, wherein said coefficient is M bits wide.

47. An apparatus according to Claim 43, wherein said selector means comprises a shift register and a multiplexer.

48. An apparatus according to Claim 47, wherein an input of said shift register is coupled to an output of said multiplexer, wherein an output of said shift register is coupled to a first input of said multiplexer, and wherein a second input of said multiplexer is coupled to an asserted signal.

49. An FIR filter according to Claim 48, further comprising:

initialization controller means for generating an initialization signal to said coefficient generator means; and

initialization wiring means for transferring the initialization signal to a selector input of said multiplexer.

50. An FIR filter according to Claim 47, wherein said shift register comprises N registers means each corresponding to a respective one of said N memory means.

51. A method of filtering a signal comprising:

(a) generating first and second coefficients;

(b) synchronizing the generation of the first and second coefficients from step (a);

(c) transferring a first control signal from step (b);

(d) transferring a second control signal from step (b);

(e) providing a shared wiring for transferring the first and second coefficients;

(f) inputting a signal;

(g) storing the first coefficient transferred in step (e) in response to said first control signal transferred in step (c);

(h) multiplying the first coefficient stored in step (g) by the signal input in step (f);

(i) delaying the signal input in step (f);

(j) storing the second coefficient transferred in step (e) in response to said second control signal transferred in step (d); and

(k) multiplying the second coefficient stored in step (j) by the signal delayed in step (i).

52. A method according to Claim 51, further comprising:

(l) generating a third coefficient,

(m) transferring a third control signal from step (b);

(n) delaying the signal from step (i);

(o) storing the third coefficient transferred in step (l) in response to said third control signal transferred in step (m); and

(p) multiplying the third coefficient stored in step (o) by the signal delayed step(n).

53. A method according to Claim 52, wherein in step (i) the signal is delayed by a first time delay, wherein in step (n) the signal is delayed by a second time delay, wherein the first time delay is equal to the second time delay.

54. A method according to Claim 52, wherein in step (i) the signal is delayed by a first time delay,

wherein in step (n) the signal is delayed by a second time delay, wherein the first time delay is different than the second time delay.

55. A method of filtering a signal comprising:

(a) generating N coefficients;

(b) providing a shared wiring for transferring the N coefficients generated in step (a);

(c)storing the N coefficients transferred in step (b);

(d) filtering an input signal responsive to the N coefficients stored step (c); and

synchronizing step (a) and step (c).

56. A method of filtering a signal comprising:

(a) generating first and second coefficients;

(b) providing shared wiring for transferring the first and second coefficients generating in step (a);

(c) inputting a signal;

(d) providing a selector signal;

(e) storing the first coefficient transferred by step (b) in response to the selector signal from step (d);

(f) multiplying the first coefficient stored in step (e) by the signal in step (c);

(g) delaying the signal input in step (c);

(h) storing the second coefficient transferred by step (b) in response to the selector signal from step (d);and

(i) multiplying the second coefficient stored in step (h) by the signal delayed in step (g).

57. A method according to Claim 56, further comprising

(j)generating a third coefficient,

(k) delaying the signal from step (g);

(l) storing the third coefficient transferred by step (b) in response to the selector signal from step (d);

(m) multiplying the third coefficient stored in step (l) by the signal delayed by step (k).

58.A method according to Claim 57, wherein in step (g) the signal is delayed by a first time delay, wherein in step (k) the signal is delayed by a second time delay, wherein the first time delay is equal to the second time delay.

59. A method according to Claim 57 wherein in step (g) the signal is delayed by a first time delay, wherein in step (k) the signal is delayed by a second time delay, wherein the first time delay is different than the second time delay.

60. A method according to Claim 56, further comprising

(n) generating an initialization signal, wherein step (a) is responsive to step (n); wherein step (d) is responsive to step (n).

61. A method of filtering a signal comprising:

(a) generating N coefficients;

(b) providing a shared wiring for transferring the N coefficients from step (a);

(c) generating a selection signal;

(d) storing the N coefficients transferred in step (b) in response to the selection generated in step (c);

(e) filtering a signal responsive to the N coefficients stored in step (d); and

(f) synchronizing step (a) with step (d).

61. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR filter comprising:

a coefficient generator to generate first and second coefficients;

a first control conductor;

a second control conductor;

a controller coupled to a first end of said first control conductor and a first end of said second control conductor;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller; and

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

62. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR apparatus having N taps, N being a positive integer of at least 2, comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said coefficient generator;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

63. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to outputting an output signal from the Ethernet cable, the output signal corresponding to the

input signal and having an echo;

an FIR filter comprising:

a coefficient generator to generate first and second coefficients;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a selector;

a first memory coupled to a second end of said shared wiring to store the first coefficient in response to said selector;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring to store the second coefficient in response to said selector;

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

64. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to output an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR filter apparatus having N taps, N being a positive integer of at least 2, comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said

coefficient generator;

a selector;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients in response to said selector; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

65. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR filter means comprising:

coefficient generator means for generating first and second coefficients;

controller means for synchronizing said coefficient generator;

first control conductor means for transferring a first control signal from said controller means;

second control conductor means for transferring a second control signal from said controller means;

shared wiring means for transferring the first and second coefficients from said coefficient generator means;

input means for inputting a signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to said first control signal transferred

by said first control conductor means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means in response to said second control signal transferred by said second control conductor means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

66. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR apparatus means having N taps, N being a positive integer of at least 2, comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

N memory means, each of said memory means responsive to said shared wiring means for storing a respective one of the N coefficients; and

FIR filter means for filtering an input signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.

67. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR filter means comprising:

coefficient generator means for generating first and second coefficients;

shared wiring means for transferring the first and second coefficients from said coefficient generator means;

input means for inputting a signal;

selector means for providing a selector signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to the selector signal from said selector means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means in response to the selector signal from said selector means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

68. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR filter apparatus means having N taps, N being a positive integer of at least 2, comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

selector means for generating a selection signal;

N memory means, each of said memory means for storing a corresponding one of the N coefficients transferred by said shared wiring means in response to the selection signal from said selector means; and

FIR filter means for filtering a signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.